WHAT IS CLAIMED IS:

1. A method of writing to a dual-port memory, the method comprising:

providing a data bit on a data line, and a complement of the data bit on a complementary data line;

selecting a word line to activate a first device coupled to the data line and a second device coupled to the complementary data line; and

selecting a column select line to activate a third device coupled between the first device and a first node of a memory cell, and a fourth device coupled between the second device and a second node of the memory cell.

2. The method of claim 1 further comprising:

before selecting the column select line, asserting a write enable.

3. The method of claim 2 further comprising:

deselecting the write enable; and

deactivating the third device and the fourth device.

4. The method of claim 3 wherein the first, second, third, and fourth devices are NMOS devices.

5. The method of claim 1 wherein the word line further couples to a read cell.

6. A method of determining the presence of a match between a data entry and a comparand in a content addressable memory, the content addressable memory comprising a plurality of memory storage cells arranged in rows and columns, each memory storage cell having a write circuit and a read circuit, wherein the write circuit and the read circuit of each memory storage cell in a row is coupled to one word line, and wherein the read cells of each memory storage cell in a column are coupled to one first read line and one second read line, the method comprising:

writing the data entry to odd numbered memory storage cells in a column of memory storage cells;

writing a complement of the data entry to even numbered memory storage cells in the column of memory storage cells;

driving word lines coupled to the even numbered memory storage cells in the column of memory storage cells with the comparand; and

driving word lines coupled to the odd numbered memory storage cells in the column of memory storage cells with a complement of the comparand.

7. The method of claim 5 further comprising:

determining a parallel impedance of the read cells in the column of memory storage cells, and outputting a match is the impedance is high.

8. The method of claim 6 further comprising decoding the position of the column of the match as a binary word.

9. The method of claim 7 wherein the data entries are product terms.

10. A method of writing to a dual-port memory comprising:

providing a data bit on a data line, and a complement of the data bit on a complementary data line;

asserting a write enable signal, which asserts a column select line thus activating a first and second device; and

asserting a word line thus activating a third and fourth device,

wherein the first and third devices are coupled between the data line and a first node of a memory cell, and the second and fourth devices are coupled between the complementary data line and a second node of the memory cell.

11. The method of claim 10 wherein a gate of the third device and a gate of the fourth device are coupled to the word line, and the third device is coupled to the data line and the fourth device is coupled to the complementary data line.

12. The method of claim 11 wherein the word line further couples to a read cell.

13. The method of claim 12 wherein a gate of the first device and a gate of the second device couple to the column select line.

14. The method of claim 13 wherein the first, second, third, and fourth devices are NMOS devices.

15. A method of reading data in a dual port memory comprising:

selecting a word line thus activating a first device; and

sensing an impedance between a first node and a second node,

wherein the first device and a second device are coupled in series between the first node and the second node, the second device having a gate coupled to a first node in a memory cell, and

wherein the word line couples to a third device and a fourth device, the third device and fourth devices used for writing to the memory cell.

16. The method of claim 15 wherein the third device couples between a data line and a fifth device and the fourth device couples between a complementary data line and a sixth device.

17. The method of claim 16 wherein the fifth device couples to the first node in the memory cell and the sixth device couples to a second node in the memory cell.

18. The method of claim 17 wherein a gate of the fifth device and a gate of the sixth device are coupled to a column select line, the column select line enabled by a write enable signal.

19. The method of claim 18 wherein the memory cell comprises a first inverter having an input and an output and a second inverter having an input and an output, the input of the first inverter coupled to the output of the second inverter, and the input of the second inverter coupled to the output of the first inverter.

20. The method of claim 15 wherein the first and second devices are NMOS devices.